Customer No.: 31561
Application No.: 10/708,371
Docket No.: 11955-US-PA

REMARKS

Present Status of the Application

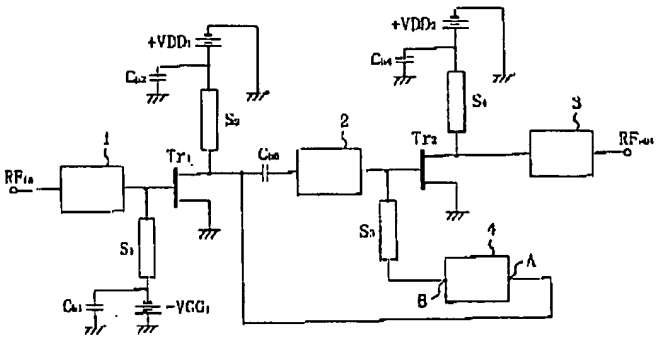
Claims 1-15 are still pending. During this response, for at least the foregoing reason, applicants respectfully submit that claims 1-15 patently define over prior art of record and reconsideration of this application is respectfully requested.

Discussion of Rejections to The Claims Under 35 U.S.C. 102(b)

The Office Action rejected presently-pending claims 1-15. Specifically, the Office Action rejected claims 1-15 under 35 U.S.C. 102, as being anticipated by Ishikawa et al. (US 5982236, hereinafter referred as Ishikawa). Reconsideration of those claims is respectfully requested.

In the Office Action, it is asserted that claims 1-15 are rejected under 35 U.S.C. 102, as being anticipated by Ishikawa. More specifically, regarding claim 1, the Office Action asserted that "Fig 5 of Ishikawa et al. disclose a power amplifier(Tr2) with an active bias circuit, comprising: a power amplifier transistor(Tr2) with a gate (gate of Tr2) connected to a gate bias voltage(B); and an active bias circuit(4) connected to an input power terminal(A) and the gate of the power amplifier transistor(gate of Tr2) for receiving an input power(output of 3) from the input power terminal(A) and outputting the gate bias voltage(B), to the gate wherein the gate bias voltage(gate of Tr2) is increased corresponding to an increase of the input power(Col.12 lines 25-30)." Applicants respectfully traverse the rejections for at least the reasons set forth below.

Fig. 5



With respect to claim 1, independent claim 1 recites the features as follows:

1. (currently amended) A power amplifier with an active bias circuit,

comprising:

a power amplifier transistor with a gate connected to a gate bias voltage ; and

an active bias circuit connected to an input power terminal and the gate of the power amplifier transistor ***for receiving an input power from the input power terminal*** and outputting the gate bias voltage to the gate,

wherein the gate bias voltage is increased corresponding to an increase of the input power. *(emphasis added)*

Ishikawa et al. does not teach "***an active bias circuit*** connected to an input power terminal and the gate of the power amplifier transistor ***for receiving an input power from the input power terminal***". As stated in col. 12, lines 25-30 of the Ishikawa reference, as followed:

> "Thus, the positive voltage generation circuit 4 detects part of the high-frequency power outputted from the output impedance matching circuit 3, outputs positive voltage which increases or decreases in accordance with an increase or decrease in the detected high-frequency power to the input terminal of the latter-stage transistor Tr2 via the third microstrip line S_3." That means the input of the positive voltage generation circuit 4 is the output of output impedance matching circuit 3, but the present invention discloses that the input power terminal and the output power terminal are different terminals. Thus, there exists a distinction between Ishikawa's teaching and applicant's teaching, whereby applicant submits that claim 1 is clearly allowable.

As stated in col. 12, lines 25-30 of the Ishikawa reference, the circuit 4 detects the RF output from the circuit 3 and then creases the positive voltage which increases or decreases in accordance with an increase or decrease in the detected high-frequency power to the input terminal of the latter-stage transistor Tr2. However, as claimed, the invention provides "an ***active bias circuit*** connected to an input power terminal and the gate of the power amplifier transistor ***for receiving an input power from the input power terminal***", the "active bias circuit" of claim 1 is used for receiving the "input power" for actively outputting the gate bias voltage to the gate, and the gate bias voltage is increased corresponding to an increase of the input power, not **the feedback manner** as stated in the Ishikawa reference. Thus, the Ishikawa reference does not anticipate claim 1, and the rejection should be withdrawn.

Regarding claim 7, as the same reasons stated above, the Ishikawa reference at

least does not disclose "*an active bias circuit connected to the power output device and the gate of the power amplifier transistor for receiving an input power from the power output device and providing a gate bias voltage to the gate*" as claimed in claim 7. Thus, the Ishikawa reference does not anticipate claim 7, and the rejection should be withdrawn.

Regarding claim 13, as the same reasons stated above, the Ishikawa reference at least does not disclose "*a method for generating a gate bias voltage of a power amplifier transistor corresponding to an input power, ... outputting a gate bias voltage* ***corresponding to the input power****, wherein the gate bias voltage is increased corresponding to an increase of the input power*" as claimed in claim 13. Thus, the Ishikawa reference does not anticipate claim 13, and the rejection should be withdrawn.

If independent claims 1,7 and 13 are allowable over the prior art of record, then its dependent claims 2-6,8-12 and 14-15 are allowable as a matter of law, because these dependent claims contain all features of their respective independent claim 1, 7 and 13.

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CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-15 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

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